LISTING OF THE CLAIMS

Claims 1-30 are pending. None of the claims have been amended. A complete listing of the current pending claims is provided below and supersedes all previous claims listing(s).

1. (Previously Presented) A method of circuit verification, comprising:

(a) performing bounded verification on a circuit design for a number of transitions, the bounded verification corresponding to a predetermined limit for a number of transitions;

(b) performing induction proof of a first property for the number of transitions, wherein the induction proof is performed by a process comprising the acts of:

including, in an inductive set of one or more states, a plurality of states of the circuit design, wherein the inductive set of one or more states includes at least states passing the first property of the circuit design;

transitioning by at least one step, in a forward direction, states of the inductive set passing at least the first property of the circuit design, resulting in transitioned states;

determining if the transitioned states of the inductive set pass at least the first property of the circuit design;

repeating at least the transitioning and the determining, until at least, the determining results in the transitioned states of the inductive set passing or failing at least the first property of the circuit design; and

(c) if the at least one property is not verified, then increasing the limit for the bounded verification and repeating from (a).

2. (Previously Presented) The method of claim 1, wherein, if all the transitioned states of the inductive set are determined to pass at least the first property of the circuit design, all the transitioned states of the inductive set determined to pass at least the first property of the circuit design were transitioned by a first total of transitions.

3. (Previously Presented) The method of claim 2, further comprising:

transitioning, in a forward direction, initial states of the circuit design by at least the first total of transitions, resulting in a forward transitioned set of states.

4. (Previously Presented) The method of claim 3, further comprising:

if the forward transitioned set of states passes the first property of the circuit design, determining the circuit design to be formally verified for at least the first property of the circuit design.

5. (Previously Presented) The method of claim 1, wherein the determining does not consider transitioned states resulting from transitioning of states of the inductive set failing at least the first property of the circuit design.

6. (Previously Presented) The method of claim 5, wherein the determining considers only transitioned states resulting from transitioning of states of the inductive set passing at least the first property of the circuit design.

7. (Previously Presented) The method of claim 1, wherein the transitioning is not performed on states of the inductive set failing at least the first property of the circuit design.

8. (Previously Presented) The method of claim 7, wherein the transitioning is performed only on states of the inductive set passing at least the first property of the circuit design.

9. (Previously Presented) The method of claim 1, wherein, each time the transitioning and the determining are repeated, prior to transitioning, the inductive set includes transitioned states.

10. (Previously Presented) The method of claim 1, wherein, each time the transitioning and the determining are repeated, prior to transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design.

11. (Previously Presented) The method of claim 1, wherein, each time the transitioning and the determining are repeated, prior to transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design.

12. (Previously Presented) A method of circuit verification, comprising:

(a) performing bounded verification on a circuit design for a number of transitions, the bounded verification corresponding to a limit for a number of transitions;

(b) performing induction proof of a first property for the number of transitions, wherein the induction proof is performed by a process comprising the acts of:

transitioning by at least one step, in a backward direction, states of an inductive set of at least one or more states of the circuit design passing at least the first property of the circuit design, resulting in transitioned states;

determining if the transitioned states of the inductive set fail at least the first property of the circuit design;

repeating the transitioning and the determining, until at least, the determining results in the transitioned states of the inductive set failing at least the first property of the circuit design; and

(c) if the at least one property is not verified, then increasing the limit for the bounded verification and repeating from (a).

13. (Previously Presented) The method of claim 12, further comprising:

a first iteration of transitioning by at least one step, in the backward direction, states of a first iteration of an inductive set of at least one or more states failing at least the first property of the circuit design, resulting in a first iteration of transitioned states.

14. (Previously Presented) The method of claim 13, further comprising:

performing a first iteration of determining if the first iteration of transitioned states of the inductive set produce at least one state failing at least the first property of the circuit design.

15. (Previously Presented) The method of claim 14, wherein, after the first iteration of transitioning, prior to the transitioning, the inductive set includes the first iteration of transitioned states.

16. (Previously Presented) The method of claim 14, wherein, after the first iteration of transitioning, prior to the transitioning, the inductive set includes the first iteration of transitioned states passing at least the first property of the circuit design.

17. (Previously Presented) The method of claim 14, wherein, after the first iteration of transitioning, prior to the transitioning, the inductive set excludes the first iteration of transitioned states failing at least the first property of the circuit design.

18. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, the determining does not consider transitioned states resulting from transitioning of states of the inductive set failing at least the first property of the circuit design.

19. (Previously Presented) The method of claim 18, wherein, at least after the first iteration of transitioning, the determining considers only transitioned states resulting from transitioning of states of the inductive set passing at least the first property of the circuit design.

20. (Previously Presented) The method of claim 19, wherein, at least after the first iteration of transitioning, the transitioning is not performed on states of the inductive set failing at least the first property of the circuit design.

21. (Previously Presented) The method of claim 20, wherein, at least after the first iteration of transitioning, the transitioning is performed only on states of the inductive set passing at least the first property of the circuit design.

22. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states.

23. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design.

24. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design.

25. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

26. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the

inductive set includes transitioned states except for transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

27. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set includes transitioned states passing at least the first property of the circuit design except for transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

28. (Previously Presented) The method of claim 12, wherein, at least after a first iteration of transitioning, each time the transitioning is repeated, prior to the transitioning, the inductive set excludes transitioned states failing at least the first property of the circuit design and transitioned states able to reach, in one forward transition, any state of the circuit design failing at least the first property.

29. (Previously Presented) A method of circuit verification, comprising:

attempting bounded verification of one or more properties of a circuit design for at least a first predetermined number of transitions;

attempting induction proof of the one or more properties of the circuit design for at least the first number of transitions; and

determining if the one or more properties of the circuit design are verified, based at least on the bounded verification and the induction proof; and

if the bounded verification and the induction proof are insufficient to determine the one or more properties of the circuit design to be verified, increasing the first predetermined number of transitions.

30. (Previously Presented) The method of claim 29, further comprising:

repeating at least one of attempting bounded verification and attempting induction proof; and

determining if the one or more properties of the circuit design are verified, based at least on repeating, with the increased first predetermined number of transitions, at least one of bounded verification and the induction proof.

31. (Cancelled).